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This certificate is awarded to

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for successfully completing the course

VLSI DESIGN FLOW: RTL TO GDS

with a consolidated score of **78%**

Online Assignments	21.53/25	Proctored Exam	55.5/75

Total number of candidates registered in this course: **6209**

Prof. Sumit J. Darak
Dean of Academic Affairs,
IIIT Delhi

JUL-OCT 2026
(12 week course)

Prof. Andrew Thangaraj
NPTEL, Coordinator
IIT MADRAS

INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

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Roll No: NPTEL26EE147S568102119 To verify the certificate No. of credits recommended: 4