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KARTHICK RATHINAM R M

for successfully completing the course

VLSI DESIGN FLOW: RTL TO GDS

with a consolidated score of **65%**

Online Assignments	21.88/25	Proctored Exam	42.75/75

Total number of candidates registered in this course: **6209**

Prof. Sumit J. Darak
Dean of Academic Affairs,
IIIT Delhi

JUL-OCT 2026
(12 week course)

Prof. Andrew Thangaraj
NPTEL, Coordinator
IIT MADRAS

INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

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